LISTING OF CLAIMS:

This listing of claims, including newly added claims 21-26, will replace all prior versions, and listings, of claims in the application:

Claim 8 (Currently Amended): A three-dimensional (3-D) integrated chip system, comprising:

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a first wafer including one or more integrated circuit (IC) devices, metallic lines deposited via an interlevel dielectric (ILD) for wafer-to-wafer bonding and electrical interconnection, and an ILD recess surrounding the metallic lines deposited via the ILD; and

a second wafer including one or more integrated circuit (IC) devices, metallic lines deposited via an interlevel dielectric (ILD) for wafer-to-wafer bonding and electrical interconnection, and an ILD recess surrounding the metallic lines deposited via the ILD,

wherein the metallic lines on the surface of the second wafer are bonded with the metallic lines on the surface of the first wafer to establish electrical connections between active IC devices on the adjacent wafers, and

wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded.

Claim 9 (Previously Added): The three-dimensional (3-D) integrated chip system as claim d in claim 8, wh r in the metallic lines include Copper (Cu)

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bonding pads deposited on opposing surface of the adjacent wafers to s rve as electrical contacts between active IC devices on both the adjacent wafers.

Claim 10 (Previously Added): The three-dimensional (3-D) integrated chip system as claimed in claim 8, wherein the ILD recess is created by a Chemical Mechanical Polish (CMP).

Claim 11 (Previously Added): The three-dimensional (3-D) integrated chip system as claimed in claim 8, wherein the ILD recess is created by selectively etching the ILD surrounding the metallic lines deposited via the ILD.

✓**Claim 12 (Cancel):**

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Claim 13 (Currently Amended)): The three-dimensional (3-D) integrated chip system as claimed in claim ~~12~~1, wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450^{0}C while the metallic lines exhibit a bonding temperature of about 400^{0}C.

Claim 14 (Currently Amended): A three-dimensional (3-D) integrated chip system, comprising:

a first wafer including one or more integrated circuit (IC) devices;

a second wafer including one or more integrated circuit (IC) devices; and

metallic lines deposited on opposing surfaces of the first and second wafers at

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designated locations with an interlevel dielectric (ILD) recess surrounding the metallic lines to facilitate direct metal bonding between the first and second wafers and establish electrical connections between active IC devices on the first and second wafers, wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded.

Claim 15 (Previously Added): The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the metallic lines include a plurality of Copper (Cu) bonding pads on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers.

Claim 16 (Previously Added): The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the ILD recess is created by a Chemical Mechanical Polish (CMP).

Claim 17 (Previously Added): The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the ILD recess is created by selectively etching the ILD surrounding the metallic lines deposited via the ILD.

Claim 18 (Cancel):

Claim 19 (Previously Added): The three-dimensional (3-D) integrated

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chip system as claimed in claim 14, wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450^{0}C while the metallic lines exhibit a bonding temperature of about 400^{0}C.

Claim 20 (Previously Added): The three-dimensional (3-D) integrated chip system as claimed in claim 14, wherein the first wafer is thinner than the second wafer to conform to height differences of the metallic lines across opposing surfaces of the adjacent wafers.

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Claim 21 (Newly Added): A chip system, comprising:

a first wafer including one or more active integrated circuit (IC) devices, and having an interlevel dielectric (ILD) deposited on a surface, and metallic lines selectively deposited, via the ILD, and settled on the surface higher than the ILD; and

a second wafer including one or more active integrated circuit (IC) devices, and having an interlevel dielectric (ILD) deposited on a surface, and metallic lines selectively deposited, via the ILD, and settled on the surface higher than the ILD;

wherein the first and second wafers are selectively aligned and bonded, via the metallic lines to establish direct metal bonding and electrical connections between active IC devices on the adjacent wafers, and

wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded.

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Claim 22 (Newly Added): The chip system as claimed in claim 21, wherein the metallic lines are Copper (Cu) bonding pads deposited on opposing surface of the first and second wafers to serve as electrical contacts between active IC devices on the first and second wafers.

Claim 23 (Newly Added): The chip system as claimed in claim 21, wherein the ILD is made recessed below the metallic lines by a Chemical Mechanical Polish (CMP).

Claim 24 (Newly Added): The chip system as claimed in claim 21, wherein the ILD is made recessed below the metallic lines by selectively etching the ILD surrounding the metallic lines deposited via the ILD.

Claim 25 (Newly Added): The chip system as claimed in claim 21, wherein the high-temperature deformable dielectric is SILK which exhibits a glass transition near 450^0C while the metallic lines exhibit a bonding temperature of about 400^0C.

Claim 26 (Newly Added): The chip system as claimed in claim 21, wherein the first wafer is thinner than the second wafer to conform to height differences of the metallic lines across opposing surfaces of the first and second wafers.